## **ELECTRONIC INFORMATION DISCLOSURE STATEMENT**

Electronic Version v18 Stylesheet Version v18.0

Title of Invention

Simulating diagonal wiring directions using manhattan directional wires

**Application Number:** 

10/043853

\*10/043853\*

**Confirmation Number:** 

9148

First Named Applicant:

Steven Teig

Attorney Docket Number: SPLX.P0007

CD1 V D0007

Art Unit:

2826

Examiner:

Alexander O. Williams

Search string:

( 5640327 or 5689433 or 5801385 or 5811863 or

5880969 or 5889329 or 6111756 or 6260183 or 6263475 or 6301686 or 6324674 or 6412097 or

6645842 or 20010009031 ).pn.

## **US Patent Documents**

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
m	1	5640327	1997-06-17	Ting			
	2	5689433	1997-11-18	Edwards			•
	3	5801385	1998-09-01	Endo et al.			
	4	5811863	1998-09-22	Rostoker et al.			
	5	5880969	1999-03-09	Hama et al.			
	6	5889329	1999-03-30	Rostoker et al.			*
	7	6111756	2000-08-29	Moresco			
	8	6260183	2001-07-10	Raspopovic et al.	Bl		
	9	6263475	2001-07-17	Toyonaga et al.	Bl		5
	10	6301686	2001-10-09	Kikuchi et al.	B1		
à	11	6324674	. 2001-11-27	Andreev et al.	B2		

Ph	12	6412097	2002-06-25	Kikuchi et al.	B1
P	13	6645842	2003-11-11	Igarashi et al.	B2

## **US Published Applications**

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
PW	1	20010009031	2001-07-19	Nitta et al.	Al		

## Signature

Examiner Name	Date
alolo bellette	10/31/09

Based on PTO/SB/08 a & b (05-03)
Approved for use through 05/31/2003. OMB 0851-0031
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40EMARK OF	Substitute for form	1449A/P	то	Application Number	10/043,853
		1001	SCUDE	Filing Date	1/11/2002
	ORMATION DI ATEMENT BY			First Named Inventor	Steven Teig
				Group Art Unit	2826
	(use as many sheets a	as neces	ssary)	Examiner Name	Alexander O. Williams
Sheet	1	of	1	Attorney Docket Number	SPLX.P0007

•		•			FOREIGN PA	ATENT DOCUMENTS		
Examiner* Initials	Cite No.1	Fo Office <sup>3</sup>		ment (ind Code if known) <sup>5</sup>	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Refevant Passages or Relevant Figures Appear	To
mi	1.	JP	04-000677		01-06-1992	Fujiwara et al.	with English translation of Abstract;	
p	2.	JP	2000-08274	3	03-21-2000	lgarashi et al.	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	1

		NON PATENT LITERATURE DOCUMENTS	
Examiner* Initials	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>6</sup>
pw	3.	Chen et al., Optimal Algorithms for Bubble Sort Based Non-Manhattan Channel Routing, May 1994, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions Volume: 13 Issues, pp. 603-609.	
	4.	Cong J. et al., DUNE – A Multilayer Gridless Routing System, May 2001, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 20, iss. 5, pp. 633-647.	
	5.	Dion J. et al., Contour: A Tile-based Gridless Router, March 1995, Digital Western Research Laboratory, research Report 95/3, pp.1-22	
	6.	Merriam-Webster's Collegiate Dictionary, 10 <sup>th</sup> edition, Merriam-Webster Incorporated, p.606	
	7.	Morton, P. B. et al., An Efficient Sequential Quadratic Programming Formulation of Optimal Wire Spacing for Cross-Talk Noise Avoidance Routing, UCSC-CRL-99-05, March 10, 1999.	
	8.	NN71091316, Use of Relatively Diagonal And Rectangular Wiring Planes n Multilayer Packages, September 1971, IBM Technical Disclosure Bulletin, Vol. No. 14, Issue No. 4, pp. 1316-1317.	
	9.	Royle, J. et al., Geometric Compaction in One Dimension for Channel Routing, 24 <sup>th</sup> ACM/IEEE Design Automation Conference, 1987, pp 140-145.	
pa	10.	Tseng H. et al., A Gridless Multilayer Router for Standard Cell Circuits Using CTM Cells, Oct. 1999, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 18, iss. 10, pp. 1462-1479.	

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This collection of information is required by 37CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing the burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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